Part f #7

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCK[redacted] MI22-1789	SERIAL NO. 09/976,624
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Werner Juengling et al.	
		FILING DATE October 12, 2001	GROUP 2813

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AI							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

EK	AJ		M. Togo et al., "A Gate-side Air-gap Structure (GAS) to Reduce the Parasitic Capacitance in MOSFETs", 1996 Symposium on VLSI Technology Digest of Technical Papers, IEEE June 1996, pgs. 38-39.
EK	AK		Anand et al., "NURA: A Feasible, Gas-Dielectric Interconnect Process", 1996 Symposium on VLSI Technology Digest of Technical Papers, IEEE June 1996, pgs. 8283.
EK	AL		Watanabe et al., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", Symposium on VLSI Technology, Issue 1993, pg. 17, 1993. Year is sufficiently early so that the month is not an issue.
EK	AM		Townsend, et al., "Silk Polymer Coating with Low Dielectric Constant and High Thermal Stability for ULSI Interlayer Dielectric", Proceedings MRS, San Francisco, CA Vol. 476, April 1997, pgs. 9-17.
EK	AN		Product Brochure and Material Safety Data Sheet, "Interlayer Dielectric", JSR Microelectronics, 12 pages, June and July 1997.

EXAMINER	Earl Kai	DATE CONSIDERED	9/28/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Part of #5
Sheet 1 of 1

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT
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ATTY. DOCKET NO.	SERIAL NO.
MI22-1789	09/976,624
APPLICANT: Werner Juengling et al.	
FILING DATE: October 12, 2001	GROUP: 2813

U.S. PATENT DOCUMENTS

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EK	AA	5,149,615	9/1992	Chakravorty et al.			
EK	AB	5,808,854	9/1998	Figura et al.			
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EK	AD	5,464,786	11/1995	Figura et al.			
EK	AE	5,654,224	8/1997	Figura et al.			
EK	AF	5,266,519	11/1993	Iwamoto			
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		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
EK	AM	EP 0 923 125 A	6/16/99	EP			✓	
EK	AN	EP 0 542 262 A	5/19/93	EP				
	AO							
	AP							
	AQ							

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EK	AR		"Monolithic Integration of 3-D Electroplated Microstructures with Unlimited Number of Levels Using Planarization with a Sacrificial Metallic Mold"; Yoon et al.; IEEE International Micro-Electro Mechanical Systems Conference; 1999; pps. 624 & 627-629.
	AS		
	AT		

EXAMINER: Eric Kim

DATE CONSIDERED: 9/28/02

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